PAPER ID-310395

Subject Code: BMC105

Roll No: | | | | | | | | | | | | | |

MCA

(SEM I) THEORY EXAMINATION 2025-26

COMPUTER ORGANIZATION & ARCHITECTURE

TIME: 3 HRS **M.MARKS: 70**

Note: Attempt all Sections. In case of any missing data; choose suitably.

SECTION A

1. Attempt *all* questions in brief. **02 x 7 = 14**

Q no.	Question	CO	Level
a.	List the functional units of a digital system.	1	K2
b.	What is a bus cycle? Give one example.	1	K3
c.	Define Booth's algorithm in one line.	1	K2
d.	What is an instruction format?	2	K2
e.	Define 2D memory organization.	3	K2
f.	What is programmed I/O?	4	K1
g.	What is SIMD also Write the full form of SIMD.	5	K1

SECTION B

2. Attempt any *three* of the following: **07 x 3 = 21**

a.	Explain signed-operand multiplication. Using Booth's algorithm, multiply –13 × +11 and show all steps.	1	K3
b.	A memory system contains 128K words and a cache of 1K blocks, each block holding 8 words. For direct mapping, determine: (i) Number of main memory blocks (ii) Word offset bits (iii) Index bits (iv) Tag bits Draw the complete physical address format.	3	K3
c.	Explain instruction cycle with neat diagrams. Write micro-operations for Fetch, Decode, and Execute phases.	2	K3
d.	Describe Flynn's classification. Compare SISD, SIMD, MISD, MIMD with suitable examples.	5	K2
e.	Explain DMA mechanism. Draw the DMA transfer timing for cycle stealing, and justify why CPU performance is affected.	4	K3

SECTION C

3. Attempt any *one* part of the following: **07 x 1 = 07**

a.	Design the architecture of a 3-bus CPU organization and illustrate how the instruction R1 ← R2 + (M[PC]) is executed using register transfer notation.	1	K3
b.	Explain the following addressing modes with examples: (i) Immediate (ii) Direct (iii) Register indirect (iv) Indexed	1	K2

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4. Attempt any *one* part of the following: **07 x 1 = 07**

a.	Design a 4-bit Carry Look-Ahead Adder and compute: $A = 1101_2$, $B = 0101_2$ Show all intermediate steps for carry generation and sum evaluation.	1	K3
b.	Convert the decimal value –19.375 into IEEE-754 single precision. Show sign, exponent, mantissa, normalization, and biasing.	1	K3

5. Attempt any *one* part of the following: **07 x 1 = 07**

a.	Describe microprogram sequencing. Explain how conditional branching is handled in a microprogrammed control unit using a sequencer diagram.	2	K4
b.	Explain pipelining. For a 5-stage pipeline, show pipeline execution of the instruction sequence: LOAD, ADD, SUB, JUMP Indicate hazards and state one solution.	2	K3

6. Attempt any *one* part of the following: **07 x 1 = 07**

a.	Explain 2½-D memory organization with a neat diagram. How does it improve access time compared to 2D organization?	3	K3
b.	Define virtual memory. Explain page fault, working set, and thrashing with examples.	3	K3

7. Attempt any *one* part of the following: **07 x 1 = 07**

a.	Explain interrupt hardware and interrupt nesting. Draw the sequence of operations during nested interrupt handling.	4	K3
b.	Explain parallel processing. Describe shared-memory MIMD and distributed-memory MIMD architectures with diagrams.	5	K2